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(54) Decoding method and apparatus for biphase coded signals

(57) A method in which a biphase coded data stream is sampled before S1 and after S2 a regular data transition (figure 4c). These samples S1, S2 are then compared to produce a decoded data output signal (figure 4i). This method overcomes problems arising where the data stream is distorted and transitions do not cross any assigned signal threshold.

The method may be implimented using a pair of sample-and-hold units, a comparator and a latch. It is applicable to Biphase Codes where regular transitions occur mid-bit (eg. Manchester II, Inverted Manchester, Biphase L), as also to Biphase Codes where regular transitions occur at end-of-bit (e.g. Manchester Mark, Manchester Space, Biphase M).

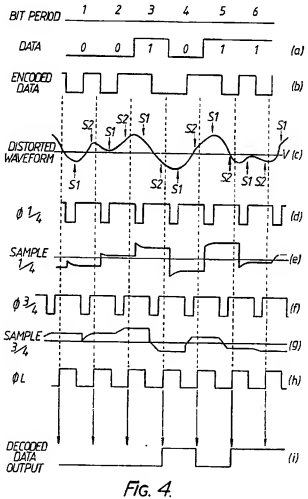


FIG. 4.

GB 2 171 277 A

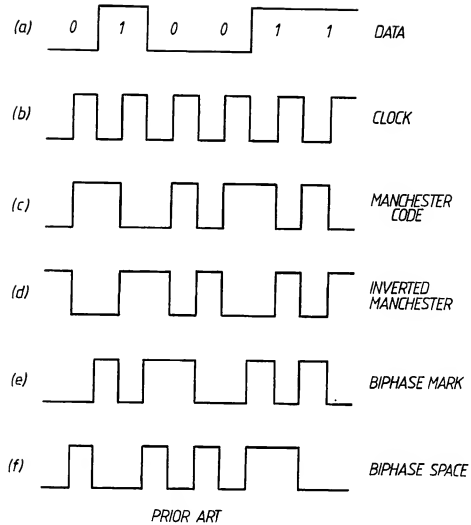
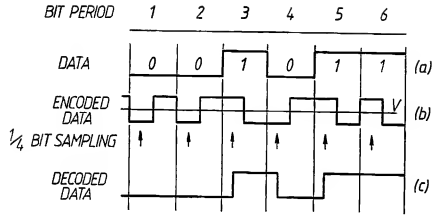
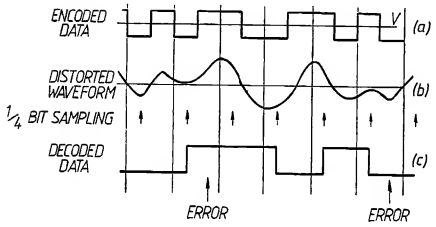

(a)
0
1
0
0
1
1
DATA
(b)
CLOCK
(c)
MANCHESTER CODE
(d)
INVERTED MANCHESTER
(e)
BIPHASE MARK
(f)
BIPHASE SPACE
PRIOR ART

FIG. 1.



PRIOR ART

FIG.2.



PRIOR ART

FIG.3.

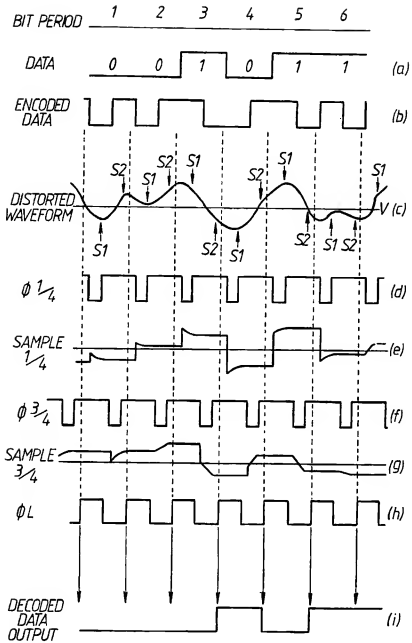

BIT PERIOD
1
2
3
4
5
6
DATA
0
0
1
0
1
1
(a)
ENCODED DATA
(b)
DISTORTED WAVEFORM
S2
S1
S2
S1
S1
S2
S1
S1
V (c)
S1
S2
S1
S2
S1
S2
φ 1/4
(d)
SAMPLE 1/4
(e)
φ 3/4
(f)
SAMPLE 3/4
(g)
φL
(h)
DECODED DATA OUTPUT
(i)

FIG. 4.

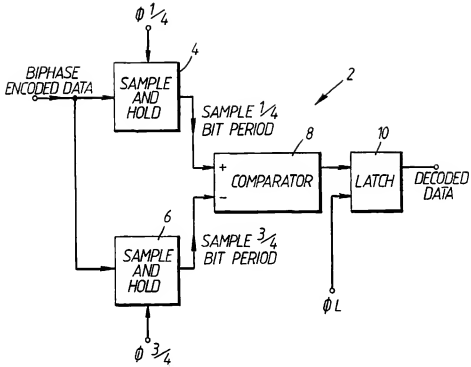

φ 1/4
4
BIPHASE ENCODED DATA
SAMPLE AND HOLD
2
SAMPLE 1/4 BIT PERIOD
8
10
+
−
COMPARATOR
LATCH
DECODED DATA
6
SAMPLE AND HOLD
SAMPLE 3/4 BIT PERIOD
φ L
φ 3/4

FIG. 5.

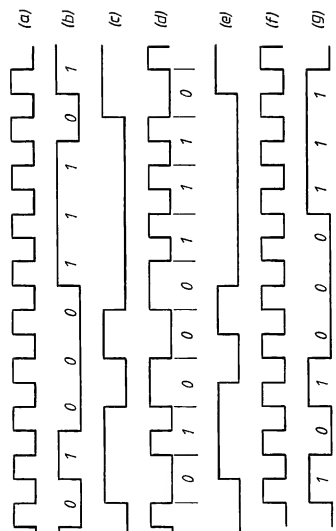

CLK
DATA
PRECODED DATA
ENCODED DATA
DECODED DATA
O/P CLK
POST-CODED DATA
(a)
(b)
(c)
(d)
(e)
(f)
(g)
1 0 1 0 0 0 1 1 1 0 1
0 1 0 0 0 1 1 1 0
1 0 1 0 0 0 1 1 1

FIG. 6.

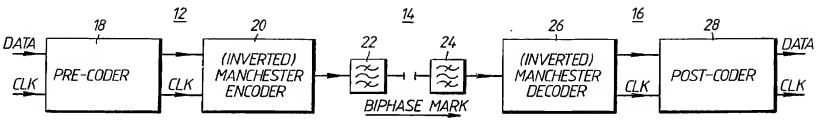


FIG. 7.

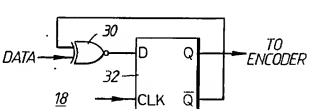


FIG. 8.

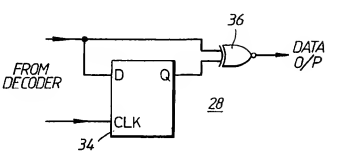


FIG. 9.

SPECIFICATION

Decoding method and apparatus for biphase coded signals

The present invention relates to a method of decoding biphase coded data streams and to apparatus therefor.

Biphase coded data streams are well known and are used extensively for the transmission of data in digital form. A biphase coded data stream may be defined as a data stream having a reguler data transition at a known point in time for each bit period of the data stream.

Examples of biphase coded data are shown in Figures 1c to f. In conventional Manchester Code (Figure 1c), data logic zero "0" is represented by a positive transition and dete logic one "1" is represented by a negative transition. In each case these "regular" transitions occur half-way through each bit period. End of bit non-regular transitions occur only when data bits are repeated. In Inverted Manchester Code (Figure 1d) data logic one "1" and zero "0" are represented by positive and negative mid-bit transitions respectively. In Biphase Mark Code (Figure 1e there is always a "regular" end-of-bit transition, data logic zero "0" is represented by no mid-bit transition and data logic one "1" is represented by a negative or positive mid-bit transition dependent on the data sequence. The last code shown, Biphese Spece Code (Figure 1f), is similar but with the representations of logic one "1" and logic zero "0" reversed.

In data transmission links it is usually necessary to pass the coded date stream through combinations of high pass or low pass filters to obtain the desired bandwith for transmission. In order to reconstruct the data transmitted in a biphase coded data stream it is known to detect zero crossings in the data stream. This may be achieved by sampling the encoded data pattern at a predetermined point in each bit period and comparing the samples with a reference. These samples are usually taken each at one querter of the time through each bit period and the samples compared directly with the reference, or at three quarters of the time through each bit period, comparing the samples with the reference and then inverting the results.

During transmission, however, some of the pulses in the data stream may become so distorted that they do not cross the reference level with which they are compared to enable decoding. If such distortion occurs errors will result in the decoded data. This distortion can be caused by the above mentioned high or low pass filters used to filter the data stream or the presence of noise or both.

It is an object of the present invention to provide a method of decoding a biphase coded data stream in which data may be extracted accurately even though the data stream mey be so distorted that the reference level is not crossed by data dependent transitions in the data stream.

Accordingly, there is provided a method of decoding a biphase coded data stream, the method comprising, for a bit period in the coded data stream, sampling the coded data stream before a regular but data dependent transition to obtain a first data sample, sampling the data stream after the data dependent transition to obtain a further data sample, and comparing the first data sample and the further data sample to decode the data.

More than one data sample may be obtained before the data dependent transition and more than one data dependent transition may be obtained after the data dependent transition. Voting logic may then be used or more complex biphase code streams decoded.

The sampling of the data stream to obtain the first and further samples may occur in the same bit period.

Preferably, the first and further data samples are held before comparison. The first sample, however, may be delayed, as altemative.

The encoded data stream may be encoded with the data dependent transition midway through the bit period. ie. The method is applicable to Manchester and Inverted Manchester coded streams and the like.

The encoded data stream may be encoded with the data dependent transition at the end of the bit period – ie. The method is also applicable to Manchester Mark and Manchester Space coded streams and the like.

Preferably, the first data sample is obtained at one quarter of the bit period of the data stream before the data dependent transition and the further data sample is obtained at one quarter of the bit period of the data stream after the data dependent transition.

The present invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 illustrates data, clock, and different biphase codes waveforms;

Figure 2 illustrates a known method of decoding a Manchester encoded data stream, the data samples being taken at one quarter of each bit period;

Figure 3 illustrates the decoding method shown in Figure 2 when applied to a distorted data stream;

Figure 4 illustrates a method of decoding a Manchester encoded data stream in accordance with the present invention;

Figure 5 illustrates a schematic block diagram of a decoder for carrying out the method shown in Figure 4;

Figure 6 illustrates signal waveforms for a Biphase Mark Code communications system;

Figure 7 illustrates such a communications system; and,

Figures 8 and *9* illustrate pre- and post- conversion circuits as may be incorporated in the communications system shown in Figure 7 preceding.

Referring to Figure 2 there is shown in Figure 2b a Manchester Biphase coded data stream representing the data shown in Figure 2a. Manchester Biphase coding represents a logicel zero in the data stream as a rising transition in the centre of a bit period and a logical one as a falling transition in the centre of a bit period. Transitions may or may not occur at the ends of the bit periods, depending upon the data pattern embodied in the data stream, as shown in Figure 2b.

In the example shown the biphase coded data stream of Figure 2b is sampled at one quarter of each bit period and the data samples obtained are compared with the reference level V. It can be seen from bit periods 1, 2 and 4 of the example shown in Figure 2 that, at the time that the data samples are taken, the voltage level of the data stream is less than the reference level V and from bit periods 3, 5 and 6 it can be seen that the voltage level of the data stream is greater than the reference level V. When these high and low voltage levels in the bit periods of data stream are compared to the reference level V they are decoded as logical ones and logical zeros respectively as the decoder is programmed to recognise that if the voltage level of any data sample taken in a bit period is high the data dependent transition in that period must be a falling transition, representing a logical one and, if the voltage level of the data sample is low in any bit period, the data dependent transition in that period must be a rising transition, representing a logical zero.

Hence, the decoded data stream is as shown in Figure 2c.

Referring now to Figure 3, there is shown in Figure 3a the encoded data stream illustrated in Figure 2. However, in view of the reasons referred to previously, the encoded data stream may be severely distorted, as shown in figure 3b. If the waveforms shown in Figures 3a and 3b are compared it can be seen that, in bit period 2 at the instant the data sample is taken, the level of the distorted waveform is greater than the reference level V whereas the level of the data waveform as encoded is less than the reference level V and hence, the data in bit period 2 is decoded as a logical one and not as a logical zero. The inverse error appears in bit period 6 in which, in view of the distortion present, the logical one in the data stream is decoded as a logical zero. Hence, in the example shown in Figure 3, the data encoded as the sequence 001011 will be decoded as the sequence 011010, as shown in Figure 3c, Similar errors might occur if the data were strobed at three quarters through the bit periods.

Referring now to Figures 4a, 4b and 4c there is shown the encoded and distorted data streams illustrated in figure 3. In the method of the present invention the data stream is sampled before and after the data dependent transition in a bit period. The example shown is Manchester Biphase coding and hence it is known that the data dependent transition occurs at a point in time midway through any bit period. The data samples in the method illustrated by Figure 4 are, therefore, taken at one quarter and three quarters through any bit period, as shown in figure 4c by the arrows S1 and S2.

Figures 4d and 4f illustrate the strobe waveforms used to sample the waveform shown in Figure 4c and Figures 4e and 4g show, respectively, the data samples obtained when the waveform of Figure 4c is strobed by the waveforms of Figures 4d and 4f.

Figure 4 shows the clock waveform used to clock the comparison of the data samples obtained at one quarter and three quarters through any bit period and Figure 4i illustrates the correctly decoded data.

In Figure 5 there is shown a decoder suitable for carrying out the method of the present invention. The decoder 2 comprises sample and hold circuits 4 and 6 for sampling the biphase encoded data stream before and after the data dependent transition in a bit period. A comparator 8 is provided for receiving output signals from the sample and hold circuits 4 and 6. The output of the comparator 8 is connected to a D-type latch 10, providing a decoded data output in response to clock pulses from a source $\emptyset_L$.

In operation, the biphase coded data stream, which may be distorted as shown in Figure 4c, is fed to the sample and hold circuits 4 and 6 of the decoder 2. The sample and hold circuit 4 is strobed by the waveform shown in Figure 4d and hence, the output from the sample and hold circuit 4 is as shown in Figure 4e. Likewise, the sample and hold circuit 6 is strobed by the waveform shown in Figure 4f and hence, the output from the sample and hold circuit 6 is as shown in Figure 4g.

Sample and hold circuits are used so as to permit the data samples obtained to stabilise before the data samples are compared in the comparator 8. The output from the comparator 8 is fed through the D-type latch 10 which is clocked by the clock waveform $\emptyset_L$ shown in figure 4h to provide the decoded data output shown in Figure 4i.

Referring now to bit periods 2 and 6 of the data stream illustrated in Figure 4, that is, the bit periods where errors would arise with known sampling methods. In bit period 2 the level of the data sample obtained by strobing at one quarter of the bit period is marginally above the reference level V.

The level of the data sample obtained by strobing at three quarters of the bit period is farther above the reference level V than that obtained at one quarter of the bit period. The respective levels of these data samples above the reference level V can be seen clearly in Figures 4e and 4g.

For bit period 2, the comparator 8 recognises that the level of the data sample taken at three quarters of that bit period is greater than the level of the data sample taken at one quarter of that bit period and interprets these levels as a rising data dependent transition, that is, a logical zero. In a like manner, the levels of the samples taken in bit period 6 are interpreted as a logical one. The comparator 8 provides an output appropriate to the interpreted data dependent transition and hence, the data embodied in the severly distorted data stream shown in Figure 4c is decoded correctly to give the decoded data output shown in Figure 4i.

Although the present invention has been described with reference to a specific embodiment it is to be understood that modifications can be effected within the scope of the invention. For example, the method has been described with respect to a biphase code having a data dependent transition in the centre of each bit period such as Manchester II code or Biphase L code. However, the method may also be applied to any type of biphase code having a data dependent transition at the end of each bit period, such as Biphase Mark, Biphase Space or Biphase M. With codes of this type one data sample would be required in one bit period and a further data sample would be required in the immediately

following bit period with the two samples being compared subsequently. However, where recovered clock is synchronised to these transitions, the adjustment would be automatic.

Furthermore, the method of the present invention need not be applied to every bit period in the data stream and also, for any bit period more than two data samples may be obtained for comparison in order to interpret any data dependent transition. Moreover, the data samples obtained may not be compared directly. The data samples which are compared in the comparator may only be dependent on the samples actually obtained, such as a fraction or a multiple of levels of the data sample obtained by strobing the encoded data stream.

To illustrate application of the invention to Biphase Mark Code decoding, consider now a typical communications link arrangement.

Such a communications link system, suited to Biphase Mark Code data signal transmission, is illustrated in Figure 7. This system comprises a transmitter section 12, a fibre link 14, and a receiver section 16. Data (figure 6b) is clocked into a preconversion circuit, precoder 18 on each cycle of the transmitter clock (figure 6a) and the output (figure 6c) of this precoder 18 relayed to an Inverted Manchester Encoder 20 and loaded on each positive clock edge. The output encoded signal (figure 6d) is then passed via a filter 22 and propagated along the fibre link 14 to the receiver 16.

Following passage of the Biphase Mark Code data stream through an input filter 24, the data is clocked into an Inverted Manchester Decoder 26 on the negative edge of a recovered clock signal (figure 6f) The decoder output signal (figure 6e) is then clocked into a post-conversion circuit, post-coder 28, and the date recovered (figure 6g).

A typical pre-coder arrangement is shown in Figure 8. This pre-coder comprises a NOR-gate 30 and e D-type latch 32. The data signal is logically combined with the inverted output $\bar{Q}$ of the latch 32, using the NOR-gate 30. Signal is extracted from the normal output Q of the latch 32 and fed to the next section of the transmitter, the encoder 20.

The Inverted Manchester Decoder 26, which includes a phase-voltage converter, also comprises sample holds 4,6, a comparator 8 and e latch 10, arranged as already shown in Figure 5. Appropriately phased clock signals are applied.

The post-coder 28 following the decoder 26 may be as shown in Figure 9. This post-conversion circuit comprises a further latch 34 and an Exclusive – NOR gate 36.

The signal output from the decoder is fed to the data input D of this latch 34 and is logically combined with the output Q signal of the latch 34, using the exclusive – NOR gate, to recover the data.

CLAIMS

1. A method of decoding a biphase coded data stream, the method comprising, for a bit period in the coded data stream, sampling the coded data stream before a regular but data dependent transition to obtain a first data sample, sampling the data stream after the data dependent transition to obtain a further data sample, and comparing the first data sample and the further data sample to decode the data.

2. A method, as claimed in claim 1, where applied to decode a Biphase Code date stream wherein each regular transition occurs mid-bit.

3. A method, as claimed in claim 1, when applied to decode a Biphase Code data stream, wherein each regular transition occurs at end-of-bit.

4. A method, as claimed in any of the preceding claims, wherein each first and further data sample is acquired one quarter of a bit period each side of the regular transition.

5. Apparatus for performing the method, as claimed in claim 1 above, comprising:-

a first and a further sample-and-hold unit;

a clock signals generator, connected to these units, to enable sampling before and after regular transition;

a comparator connected to receive samples held by the sample-and hold units; and,

a latch, connected to receive output signal from the comparator, and connected to the generator, to be enabled following acquisition of each further data sample.

6. Apparatus, as claimed in claim 5, when combined with a post-conversion circuit comprising a latch and an Exclusive NOR – gate.

7. A method of decoding a Biphase Coded data stream when performed substantially as described hereinbefore with reference to the Figures 4 and 5, or 5, 6, 7, 8 and 9 of the accompanying drawings.

8. Apparatus, for decoding a Biphase Coded data stream, constructed, adapted and arranged to operate substantially as described hereinbefore with reference to and as shown in Figures 4 and 5, or, 5, 6, 7, 8 and 9 of the accompanying drawings.

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